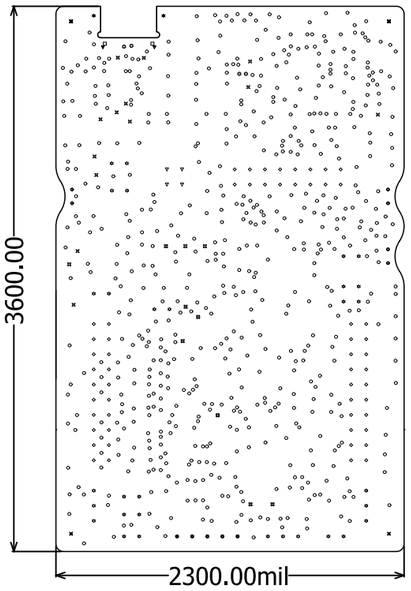
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 High Tg	8.00mil	4.2	
5	Signal Layer 1	Copper	1.40mil		
6	Dielectric 2	FR-4 High Tg	40.00mil	4.2	
7	Signal Layer 2	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	8.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
⊠	6	35.43mil (0,900mm)	NPTH	Round	Top Layer - Bottom Layer	
○	2	118.11mil (3,000mm)	NPTH	Round	Top Layer - Bottom Layer	+/-0,00mil
□	4	125,00mil (3,175mm)	NPTH	Round	Top Layer - Bottom Layer	
✖	4	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
✱	33	9.84mil (0.250mm)	PTH	Round	Top Layer - Bottom Layer	
✿	7	15.75mil (0.400mm)	PTH	Round	Top Layer - Bottom Layer	
⌘	8	25.00mil (0.635mm)	PTH	Round	Top Layer - Bottom Layer	
▽	56	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
✪	5	43.31mil (1.100mm)	PTH	Round	Top Layer - Bottom Layer	+/-1.97mil
◇	4	43.31mil (1.100mm)	PTH	Round	Top Layer - Bottom Layer	
✲	27	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
◙	2	27.56mil (0.700mm)	PTH	Slot	Top Layer - Bottom Layer	
▼	2	59.06mil (1.500mm)	PTH	Slot	Top Layer - Bottom Layer	
◎	2	74.80mil (1.900mm)	PTH	Slot	Top Layer - Bottom Layer	
	162 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 7.874 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-4 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☐ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: LP-AM13E230
DESIGNED FOR: Public Release
FILE NAME: MCU178E2.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: MCU178	REV: E2	SVN REV: Not in version control
LAYER NAME = [illegible]	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 2/19/2026 9:39:42 AM	TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
Brennan Hartigan	Lierda
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.1.1.15